

# CSD19535KTT 100 V N-Channel NexFET™ Power MOSFET

## 1 Features

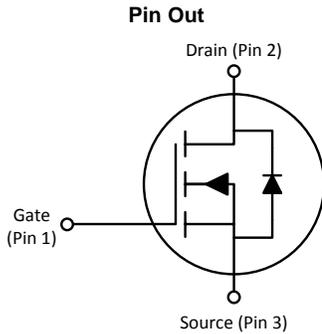
- Ultra-Low  $Q_g$  and  $Q_{gd}$
- Low Thermal Resistance
- Avalanche Rated
- Pb-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- D<sup>2</sup>PAK Plastic Package

## 2 Applications

- Hot Swap
- Motor Control
- Secondary Side Synchronous Rectifier

## 3 Description

This 100 V, 2.8 mΩ, D<sup>2</sup>PAK (TO-263) NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



## Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
$V_{DS}$	Drain-to-Source Voltage	100		V
$Q_g$	Gate Charge Total (10 V)	75		nC
$Q_{gd}$	Gate Charge Gate-to-Drain	11		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 6\text{ V}$	3.2	mΩ
		$V_{GS} = 10\text{ V}$	2.8	mΩ
$V_{GS(th)}$	Threshold Voltage	2.7		V

## Ordering Information<sup>(1)</sup>

Device	Qty	Media	Package	Ship
CSD19535KTT	500	13-Inch Reel	D <sup>2</sup> PAK Plastic Package	Tape & Reel
CSD19535KTTT	50			

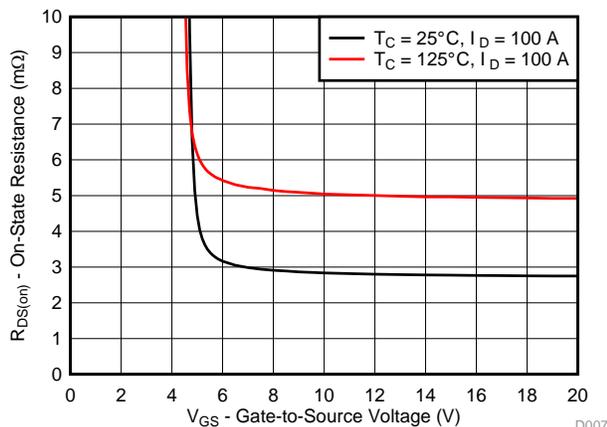
(1) For all available packages, see the orderable addendum at the end of the data sheet.

## Absolute Maximum Ratings

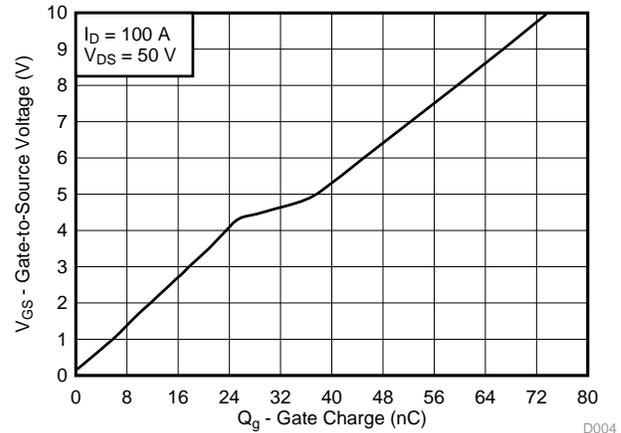
$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	100	V
$V_{GS}$	Gate-to-Source Voltage	±20	V
$I_D$	Continuous Drain Current (Package limited)	200	A
	Continuous Drain Current (Silicon limited), $T_C = 25^\circ\text{C}$	197	
	Continuous Drain Current (Silicon limited), $T_C = 100^\circ\text{C}$	139	
$I_{DM}$	Pulsed Drain Current <sup>(1)</sup>	400	A
$P_D$	Power Dissipation, $T_C = 25^\circ\text{C}$	300	W
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range	-55 to 175	°C
$E_{AS}$	Avalanche Energy, single pulse $I_D = 95\text{ A}, L = 0.1\text{ mH}$	451	mJ

(1)  $R_{\theta JC} = 0.5^\circ\text{C/W}$ , Pulse duration  $\leq 100\ \mu\text{s}$ , Duty cycle  $\leq 1\%$ .

**$R_{DS(on)}$  vs  $V_{GS}$**



**Gate Charge**



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## 4 Revision History

DATE	REVISION	NOTES
March 2015	*	Initial release.

## 5 Specifications

### 5.1 Electrical Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
$V_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	100			V
$I_{DSS}$	Drain-to-Source Leakage Current	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.2	2.7	3.4	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 6\text{ V}, I_D = 100\text{ A}$		3.2	4.1	m $\Omega$
		$V_{GS} = 10\text{ V}, I_D = 100\text{ A}$		2.8	3.4	m $\Omega$
$g_{fs}$	Transconductance	$V_{DS} = 10\text{ V}, I_D = 100\text{ A}$		301		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}, f = 1\text{ MHz}$		6100	7930	pF
$C_{oss}$	Output Capacitance			1160	1510	pF
$C_{rss}$	Reverse Transfer Capacitance			29	38	pF
$R_G$	Series Gate Resistance			1.4	2.8	$\Omega$
$Q_g$	Gate Charge Total (10 V)	$V_{DS} = 50\text{ V}, I_D = 100\text{ A}$		75	98	nC
$Q_{gd}$	Gate Charge Gate-to-Drain			11		nC
$Q_{gs}$	Gate Charge Gate-to-Source			25		nC
$Q_{g(th)}$	Gate Charge at $V_{th}$			16		nC
$Q_{oss}$	Output Charge	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		210		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 50\text{ V}, V_{GS} = 10\text{ V}, I_{DS} = 100\text{ A}, R_G = 0\ \Omega$		9		ns
$t_r$	Rise Time			18		ns
$t_{d(off)}$	Turn Off Delay Time			21		ns
$t_f$	Fall Time			15		ns
<b>DIODE CHARACTERISTICS</b>						
$V_{SD}$	Diode Forward Voltage	$I_{SD} = 100\text{ A}, V_{GS} = 0\text{ V}$		0.9	1.1	V
$Q_{rr}$	Reverse Recovery Charge	$V_{DS} = 50\text{ V}, I_F = 100\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		435		nC
$t_{rr}$	Reverse Recovery Time			85		ns

### 5.2 Thermal Information

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance			0.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance			62	

### 5.3 Typical MOSFET Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

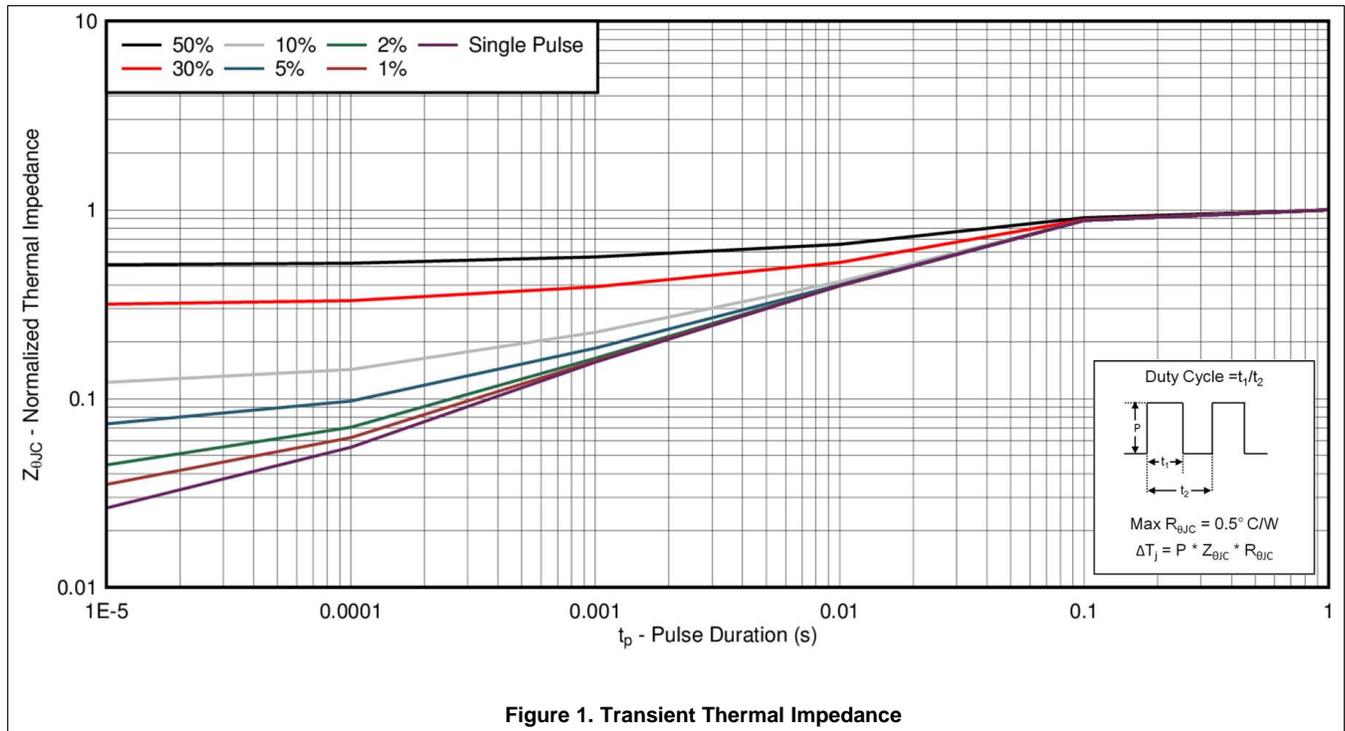


Figure 1. Transient Thermal Impedance

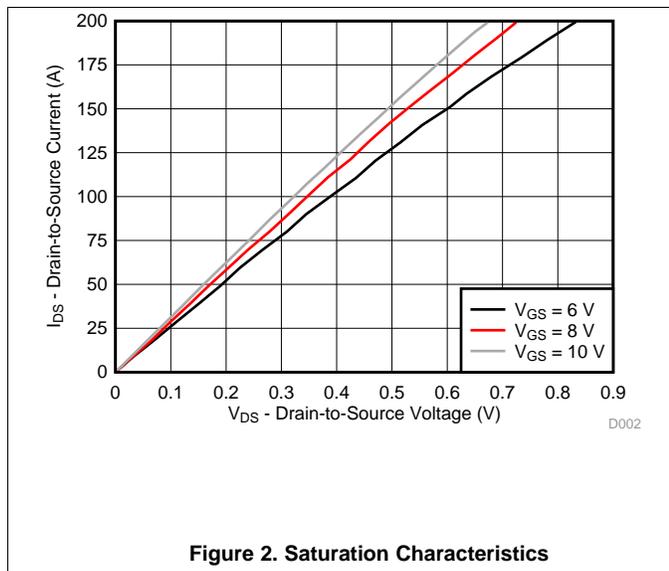


Figure 2. Saturation Characteristics

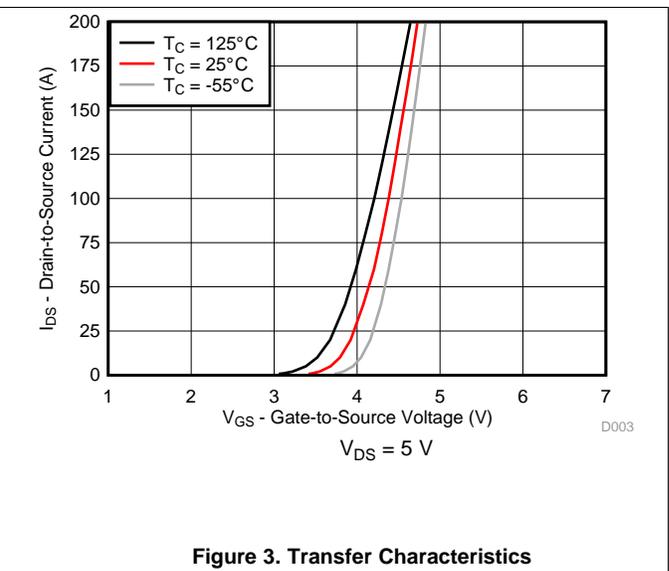


Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

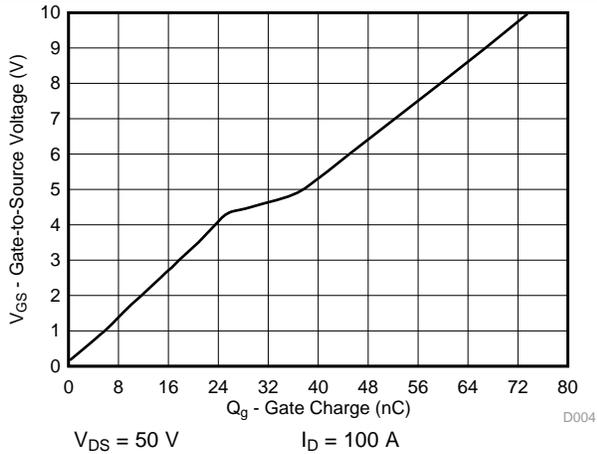


Figure 4. Gate Charge

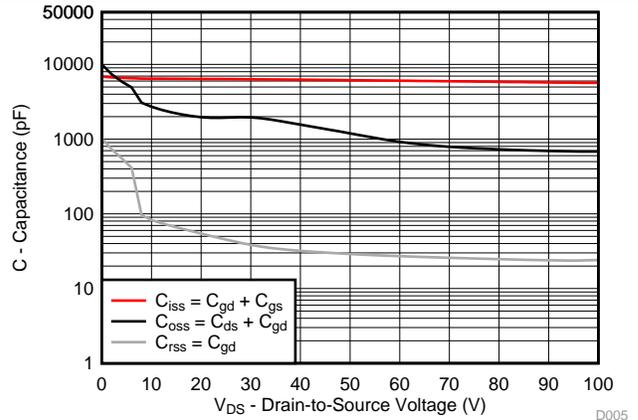


Figure 5. Capacitance

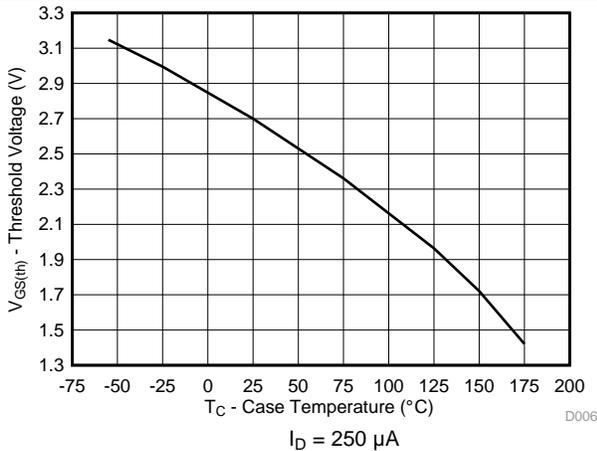


Figure 6. Threshold Voltage vs Temperature

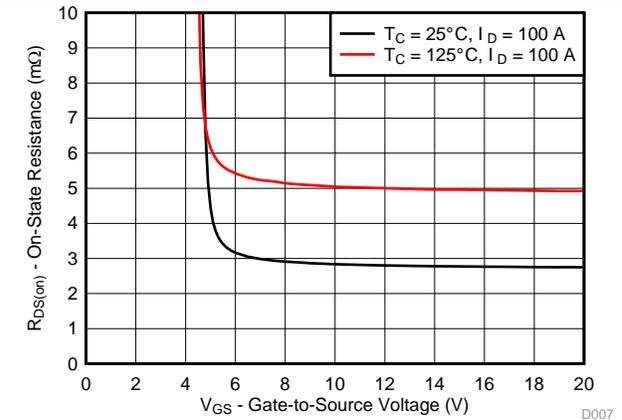


Figure 7. On-State Resistance vs Gate-to-Source Voltage

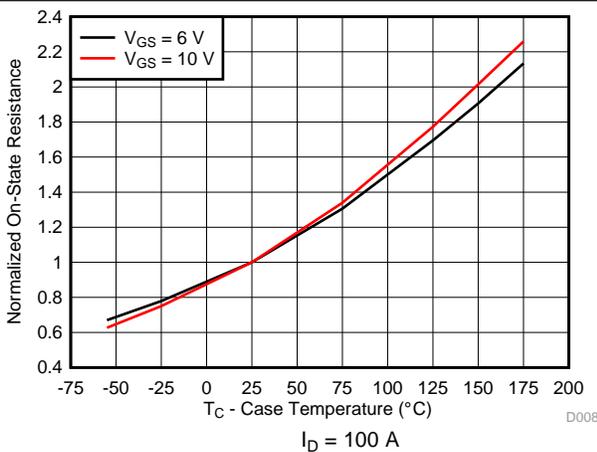


Figure 8. Normalized On-State Resistance vs Temperature

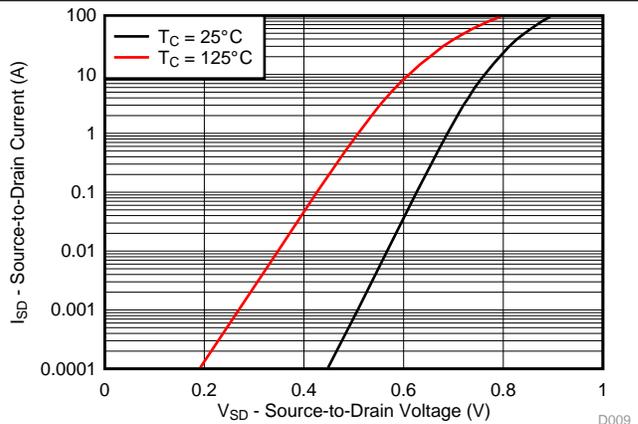
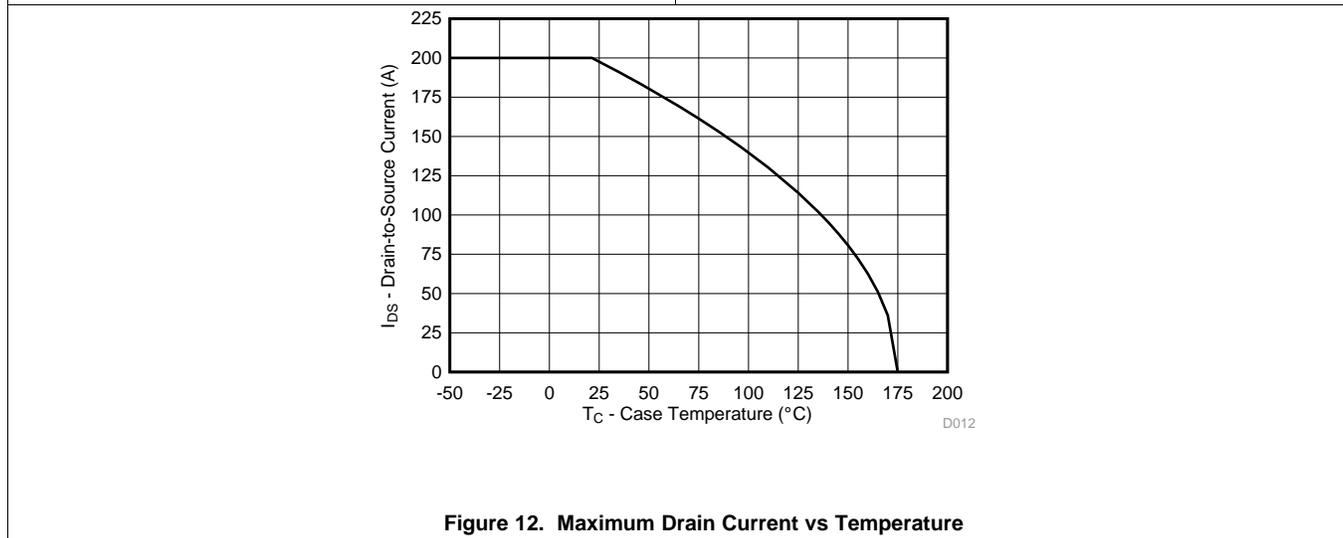
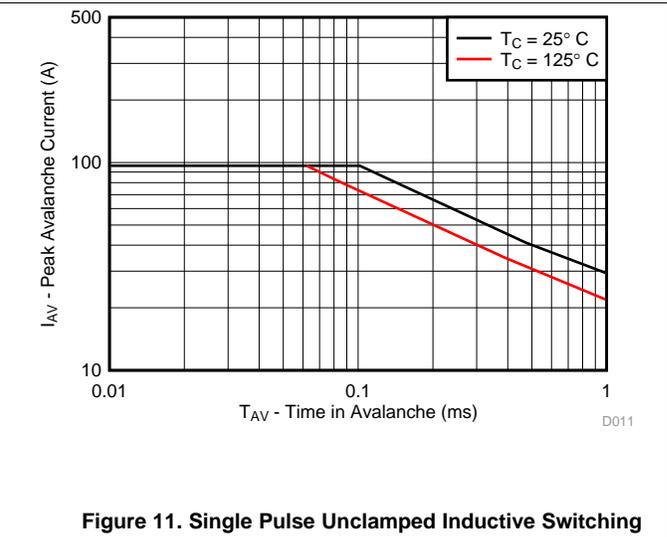
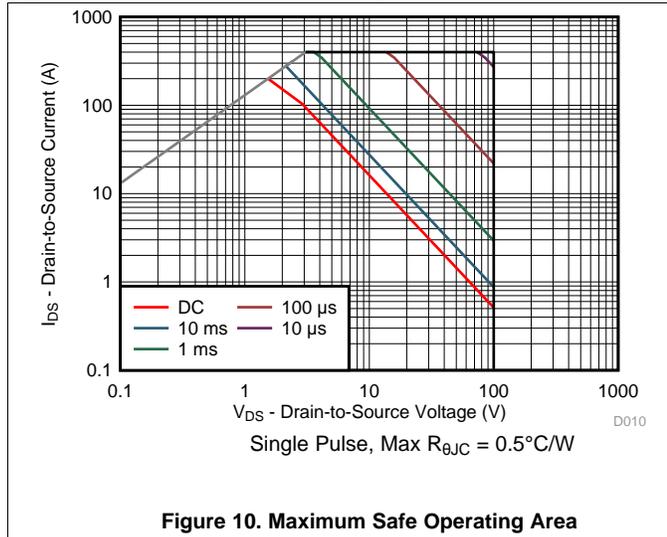


Figure 9. Typical Diode Forward Voltage

**Typical MOSFET Characteristics (continued)**

( $T_A = 25^\circ\text{C}$  unless otherwise stated)



## 6 Device and Documentation Support

### 6.1 Trademarks

NexFET is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.3 Glossary

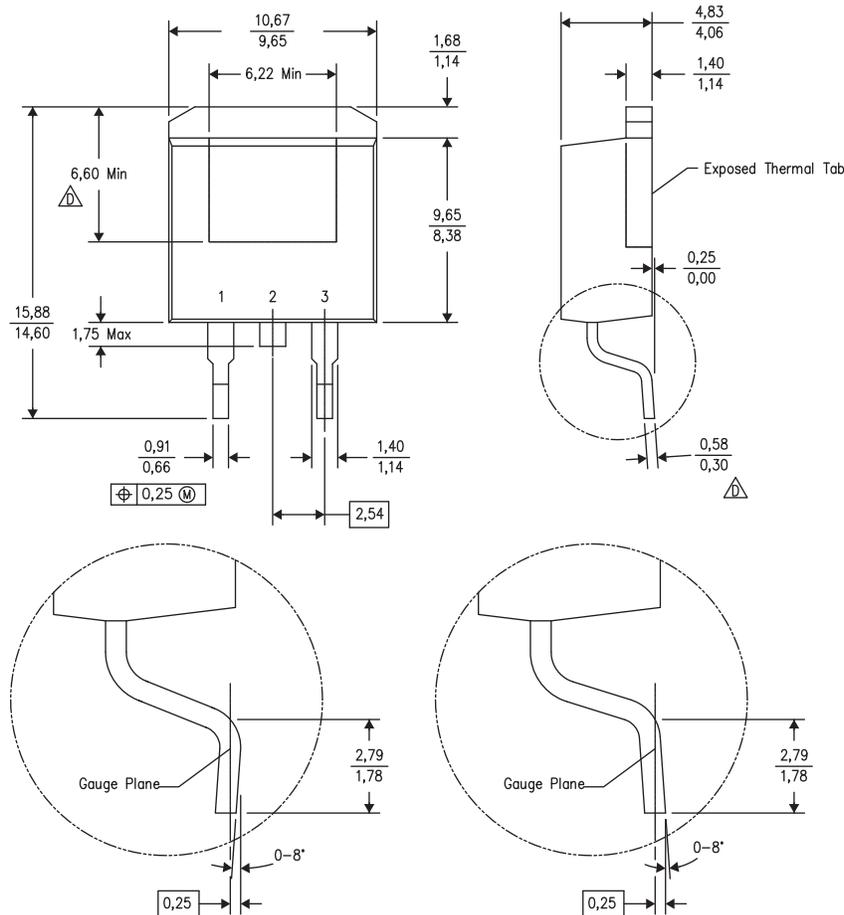
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 KTT Package Dimensions



#### Notes:

1. All linear dimensions are in inches
2. This drawing is subject to change without notice
3. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005mm per side.
4. "D" Falls within JEDEC TO-263 variation AB, except minimum lead thickness and minimum exposed pad length.

#### Pin Configuration

Position	Designation
Pin 1	Gate
Pin 2 / Tab	Drain
Pin 3	Source

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD19535KTT	PREVIEW	DDPAK/ TO-263	KTT	3	500	Pb-Free (RoHS Exempt)	CU SN	Level-2-260C-1 YEAR		CSD19535KTT	
CSD19535KTTT	PREVIEW	DDPAK/ TO-263	KTT	3	50	TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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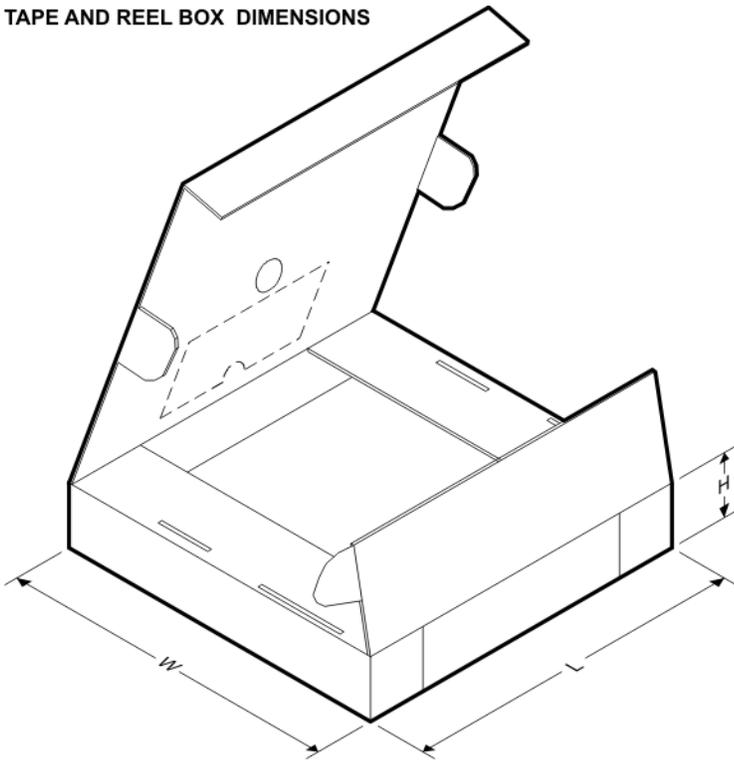
**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD19535KTT	DDPAK/ TO-263	KTT	3	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2

**TAPE AND REEL BOX DIMENSIONS**

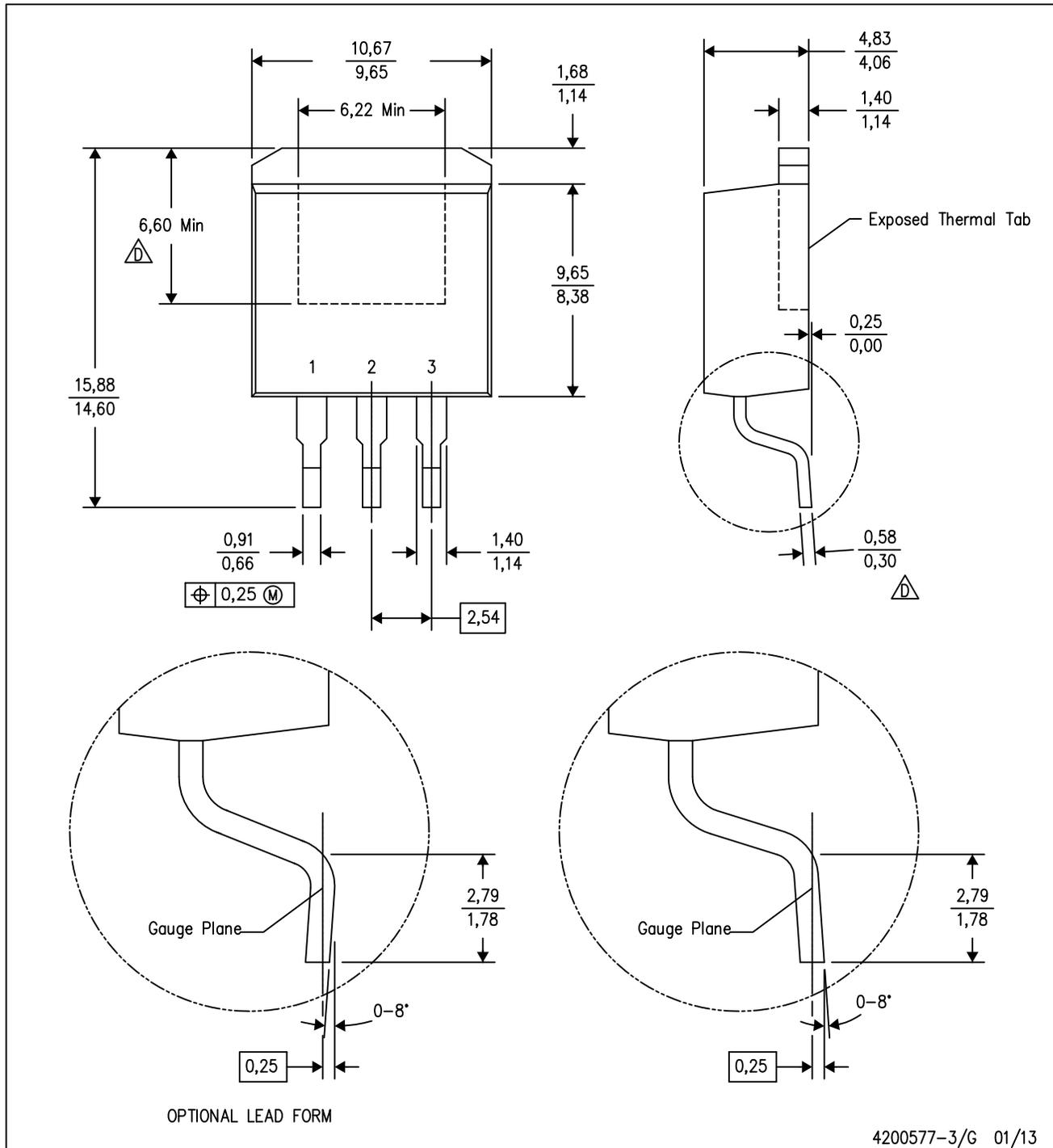


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD19535KTT	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0

KTT (R-PSFM-G3)

PLASTIC FLANGE-MOUNT PACKAGE



4200577-3/G 01/13

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
- Falls within JEDEC TO-263 variation AA, except minimum lead thickness and minimum exposed pad length.

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Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
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RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
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Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
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